IN THE CLAIMS

1. (currently amended) A memory array comprising:

two or more layers of memory material, each layer of memory material comprising an array of memory cells; ~~and~~

a first contact penetrating through each layer of memory material in a first plane and electrically connected to each layer of memory material so as to electrically interconnect the layers of memory material in the first plane; and

a second contact penetrating through each of the layers of memory material in a second plane substantially perpendicular to the first plane so as to electrically interconnect the layers of memory material in the second plane.

2. (original) The memory array of claim 1, further comprising a dielectric layer disposed between successive layers of memory material.

3. (currently amended) A memory array comprising:

two or more layers of memory material, each layer of memory material comprising an array of memory cells;

a first contact penetrating through each layer of memory material in a first plane and electrically connected to each layer of memory material so as to electrically interconnect the layers of memory material in the first plane;

~~The memory array of claim 1, further comprising:~~

a select transistor disposed on a substrate of the memory array below the layers of memory material; and

a conductive plug connecting a first source/drain region of the select transistor to a conductive layer located above the layers of memory material, wherein a second source/drain region of the select transistor is connected to the first contact.

4. (canceled)

5. (currently amended) The memory array of claim [[4]] 1, further comprising:

a select transistor disposed on a substrate of the memory array below the layers of memory material; and

a conductive plug connecting a first source/drain region of the select transistor to a conductive layer located above the layers of memory material, wherein a second source/drain region of the select transistor is connected to the second contact.

6. (currently amended) The memory array of claim [[4]] 1, further comprising a select transistor disposed on each layer of memory material between the memory cells and the second contact.

7. (withdrawn-currently amended) The memory array of claim 1, further comprising:

~~a second contact penetrating through one of the layers of memory material in a second plane substantially perpendicular to the first plane and electrically connected thereto; and~~

a third contact penetrating through another of the layers of memory material in the second plane and electrically connected thereto.

8. (withdrawn) The memory array of claim 7, further comprising:

first and second select transistors disposed on a substrate of the memory array below the layers of memory material;

a first conductive plug connecting a first source/drain region of the first select transistor to a conductive layer located above the layers of memory material, wherein a second source/drain region of the first select transistor is connected to the second contact; and

a second conductive plug connecting a first source/drain region of the second select transistor to the conductive layer located above the layers of memory material,

wherein a second source/drain region of the second select transistor is connected to the third contact.

9. (original) The memory array of claim 1, wherein each of the memory cells is a floating gate transistor.

10. (original) The memory array of claim 1, wherein each of the memory cells is a silicon-on-sapphire transistor, silicon-on-insulator transistor, thin film transistor, thermoelectric polymer transistor, or silicon-oxide-nitride-oxide-silicon transistor.

11. (withdrawn) The memory array of claim 1, wherein each array of memory cells is a NAND flash memory array or a NOR flash memory array.

12. (original) The memory array of claim 1, wherein the memory array is a read only memory array or a static random access memory array.

13. (original) The memory array of claim 1, wherein the layers of memory material comprise polysilicon.

14. (original) A memory array comprising:

a plurality of layers of memory material, each layer of memory material containing an array of memory cells arranged in rows and columns and each of the plurality of layers of memory material separated from each other by a dielectric material;

a plurality of first contacts passing through each of the plurality of layers of memory material, each first contact in electrical communication with at least one memory cell of a column of memory cells in each of the plurality of layers of memory material;

a plurality of second contacts passing through each of the plurality of layers of memory material, each second contact in selective electrical communication with a row of memory cells in each of the plurality of layers of memory material; and

a plurality of first select transistors, each first select transistor connected between a second contact and its respective row of memory cells for providing selective electrical communication, the plurality of first select transistors adapted to provide electrical communication with only one row of memory cells for each second contact.

15. (original) The memory array of claim 14, further comprising for each first contact:

one second select transistor disposed on a substrate of the memory array below the layers of memory material; and

one first conductive plug passing through the memory array and connecting a first source/drain region of the second select transistor to a global bit line located above the layers of memory material, wherein a second source/drain region of the second select transistor is connected to the first contact.

16. (original) The memory array of claim 15, further comprising for each second contact:

one third select transistor disposed on the substrate below the layers of memory material; and

one second conductive plug connecting a first source/drain region of the third select transistor to a global row line located above the layers of memory material, wherein a second source/drain region of the third select transistor is connected to the second contact.

17. (original) The memory array of claim 14, wherein each of the memory cells is a flash memory cell.

18. (original) The memory array of claim 14, wherein each of the memory cells is a silicon-on-sapphire transistor, silicon-on-insulator transistor, thin film transistor, thermoelectric polymer transistor, or silicon-oxide-nitride-oxide-silicon transistor.

19. (withdrawn) The memory array of claim 14, wherein the array of memory cells of each layer of memory material is a NAND flash memory array or a NOR flash memory array.

20. (original) The memory array of claim 14, wherein the memory array is a read only memory array or a static random access memory array.

21. (original) The memory array of claim 14, further comprising a plurality of second select transistors, each second select transistor connected between a first contact and its respective column of memory cells for providing selective electrical communication, wherein each first contact is connected directly to a global bit line located above the layers of memory material.

22. (original) The memory array of claim 14, wherein each second contact is connected directly to a global row line located above the layers of memory material.

23. (withdrawn) The memory array of claim 14, wherein each first contact electrically connects NAND strings of the respective layers of memory material.

24. (withdrawn) The memory array of claim 14, wherein each first contact electrically connects drain regions of memory cells of the respective layers of memory material.

25. (original) A memory array comprising:

a plurality of layers of memory material, each layer of memory material containing an array of memory cells arranged in rows and columns and each of the plurality of layers of memory material separated from each other by a dielectric material;

a plurality of first contacts passing through each of the plurality of layers of memory material, each first contact in electrical communication with at least one memory cell of a row of memory cells in each of the plurality of layers of memory material;

a plurality of second contacts passing through each of the plurality of layers of memory material, each second contact in selective electrical communication with a column of memory cells in each of the plurality of layers of memory material; and

a plurality of first select transistors, each first select transistor connected between a second contact and its respective column of memory cells for providing selective electrical communication, the plurality of first select transistors adapted to provide electrical communication with only one column of memory cells for each second contact.

26. (original) The memory array of claim 25, further comprising for each first contact:

one second select transistor disposed on a substrate of the memory array below the layers of memory material; and

one first conductive plug connecting a first source/drain region of the second select transistor to a global row line located above the layers of memory material, wherein a second source/drain region of the second select transistor is connected to the first contact.

27. (original) The memory array of claim 26, further comprising for each second contact:

one third select transistor disposed on the substrate below the layers of memory material; and

one second conductive plug connecting a first source/drain region of the third select transistor to a global bit line located above the layers of memory material, wherein a second source/drain region of the third select transistor is connected to the second contact.

28. (original) The memory array of claim 25, further comprising a plurality of second select transistors, each second select transistor connected between a first contact and its respective row of memory cells for providing selective electrical communication, wherein each first contact is connected directly to a global row line located above the layers of memory material.

29. (original) The memory array of claim 25, wherein each second contact is connected directly to a global bit line located above the layers of memory material.

30. (original) The memory array of claim 25, wherein each of the memory cells is a flash memory cell.

31. (original) The memory array of claim 25, wherein each of the memory cells is a silicon-on-sapphire transistor, silicon-on-insulator transistor, thin film transistor, thermoelectric polymer transistor, or silicon-oxide-nitride-oxide-silicon transistor.

32. (withdrawn) The memory array of claim 25, wherein the array of memory cells of each layer of memory material is a NAND flash memory array or a NOR flash memory array.

33. (original) The memory array of claim 25, wherein the memory array is a read only memory array or a static random access memory array.

34. (withdrawn) The memory array of claim 25, wherein the second contact electrically connects NAND strings of the respective layers of memory material.

35. (withdrawn) The memory array of claim 25, wherein the second contact electrically connects drain regions of memory cells of the respective layers of memory material.

36-95 (canceled)

96. (original) A memory device comprising:

a multi-layer memory array, wherein the array comprises:

a plurality of layers of memory material, each layer of memory material containing an array of memory cells arranged in rows and columns and each of the plurality of layers of memory material separated from each other by a dielectric material;

a plurality of first contacts passing through each of the plurality of layers of memory material, each first contact in electrical communication with at least one memory cell of a column of memory cells in each of the plurality of layers of memory material;

a plurality of second contacts passing through each of the plurality of layers of memory material, each second contact in selective electrical communication with a row of memory cells in each of the plurality of layers of memory material;

a plurality of first select transistors, each first select transistor connected between a second contact and its respective row of memory cells for providing selective electrical communication, the plurality of first select transistors adapted to provide electrical communication with only one row of memory cells for each second contact; and

a plurality of global bit lines and global row lines above the layers of memory material, each global bit line in electrical communication with at least one

of the first contacts and each global row line in electrical communication with at least one of the second contacts;

column access circuitry connected to the plurality of global bit lines; and

row access circuitry connected to the plurality of global row lines.

97. (original) A memory device comprising:

a multi-layer memory array, wherein the array comprises:

a plurality of layers of memory material, each layer of memory material containing an array of memory cells arranged in rows and columns and each of the plurality of layers of memory material separated from each other by a dielectric material;

a plurality of first contacts passing through each of the plurality of layers of memory material, each first contact in electrical communication with at least one memory cell of a row of memory cells in each of the plurality of layers of memory material;

a plurality of second contacts passing through each of the plurality of layers of memory material, each second contact in selective electrical communication with a column of memory cells in each of the plurality of layers of memory material;

a plurality of first select transistors, each first select transistor connected between a second contact and its respective column of memory cells for providing selective electrical communication, the plurality of first select transistors adapted to provide electrical communication with only one column of memory cells for each second contact; and

a plurality of global bit lines and global row lines above the layers of memory material, each global bit line in electrical communication with at least one of the second contacts and each global row line in electrical communication with at least one of the first contacts;

column access circuitry connected to the plurality of global bit lines; and

row access circuitry connected to the plurality of global row lines.

98-99 (canceled)

100. (original) An electronic system comprising:

a processor;

a memory device connected to the processor, the memory device comprising:

a multi-layer memory array, wherein the memory array comprises:

a plurality of layers of memory material, each layer of memory material containing an array of memory cells arranged in rows and columns and each of the plurality of layers of memory material separated from each other by a dielectric material;

a plurality of first contacts passing through each of the plurality of layers of memory material, each first contact in electrical communication with at least one memory cell of a column of memory cells in each of the plurality of layers of memory material;

a plurality of second contacts passing through each of the plurality of layers of memory material, each second contact in selective electrical communication with a row of memory cells in each of the plurality of layers of memory material;

a plurality of first select transistors, each first select transistor connected between a second contact and its respective row of memory cells for providing selective electrical communication, the plurality of first select transistors adapted to provide electrical communication with only one row of memory cells for each second contact; and

a plurality of global bit lines and global row lines above the layers of memory material, each global bit line in electrical communication with at least one of the first contacts and each global row line in electrical communication with at least one of the second contacts;

column access circuitry connected to the plurality of global bit lines; and

row access circuitry connected to the plurality of global row lines.

101. (original) An electronic system comprising:

a processor;

a memory device connected to the processor, the memory device comprising:

a multi-layer memory array, wherein the memory array comprises:

a plurality of layers of memory material, each layer of memory material containing an array of memory cells arranged in rows and columns and each of the plurality of layers of memory material separated from each other by a dielectric material;

a plurality of first contacts passing through each of the plurality of layers of memory material, each first contact in electrical communication with at least one memory cell of a row of memory cells in each of the plurality of layers of memory material;

a plurality of second contacts passing through each of the plurality of layers of memory material, each second contact in selective electrical communication with a column of memory cells in each of the plurality of layers of memory material;

a plurality of first select transistors, each first select transistor connected between a second contact and its respective column of memory cells for providing selective electrical communication, the plurality of first select transistors adapted to provide electrical communication with only one column of memory cells for each second contact; and

a plurality of global bit lines and global row lines above the layers of memory material, each global bit line in electrical communication with at least one of the second contacts and each global row line in electrical communication with at least one of the first contacts;

column access circuitry connected to the plurality of global bit lines; and

row access circuitry connected to the plurality of global row lines.

102-103 (canceled)